

Atty. Docket No. PLA31221/DBE/US
Serial No: 10/751,200

Remarks

Applicant and his representatives have carefully reviewed the Office Action dated June 13, 2005 ("OA2"). We note that Claim 1, rejected by Examiner Luu, was amended in the response of March 30, 2005 to include the limitations of Claim 4, which Examiner Luu had previously indicated was allowable subject matter in the Office Action of December 30, 2004. We assume that the proper procedures for rejecting previously allowed subject matter, including the step of submitting the rejection to the primary examiner for consideration of all the facts and approval of the proposed action, have been followed. (See MPEP § 706.04.)

The present invention relates to a method for packaging a multi-chip module, including the steps of (a) connecting connection terminals of a tape of an anisotropic conductive adhesive film, on which a circuit is patterned, to bond pads of a chip by applying a first anisotropic conductive adhesive on the tape and using a first C4 process, (b) applying an adhesive on an upper surface of the chip, folding the tape and attaching the folded tape to the upper surface of the chip, (c) forming a plurality of ball terminals on a lower surface of the tape, the ball terminals being electrically connected to the connection terminals of the tape, (d) manufacturing a plurality of individual chip scale packages by repeating the steps (a) to (c), and (e) laminating the individual chip scale packages, wherein the ball terminals of an upper individual chip scale package are electrically connected to the circuit on an outer surface of the tape which covers a lower individual chip scale package.

The Rejection of Claims 1-2 and 5-12 under 35 U.S.C. § 103(a)

The rejection of Claims 1-2 and 5-12 under 35 U.S.C. § 103(a) as being unpatentable over Mukerji (US 6,300,679) in view of Crafts (US 5,492,235) is respectfully traversed.

Mukerji relates to a semiconductor device, including a tape 120 formed from an electrically insulative substrate (see, e.g., Mukerji, col. 2, ll. 12-14) with a layer of electrically conductive material or traces thereon. The tape disclosed by Mukerji is neither anisotropically conductive nor adhesive. Mukerji further discloses forming traces and vias on and through the

Atty. Docket No. PIA31221/DBE/US
Serial No: 10/751,200

tape (see, e.g., Mukerji, col. 2, ll. 23-29 and 34-35), attaching a semiconductor chip to the tape (see, e.g., cols. 2-3, ll. 64-4), and using solder to electrically couple the chip to the tape (see, e.g., Mukerji, col. 3, ll. 7-11). Mukerji fails to teach or suggest a step of attaching the chip to an anisotropic conductive adhesive film the using a controlled collapse chip connection (C4) process after first applying an anisotropic conductive adhesive on the tape. Mukerji further discloses the formation of electrical interconnect structures in the vias (see, e.g., Mukerji, col. 3, ll. 37-41). Thus Mukerji teaches the formation of electrical terminals *through vias in the insulative film*, and therefore fails to teach or suggest forming ball terminals *on the surface of a* tape of an anisotropic conductive adhesive film. Finally, Mukerji discloses that at least two tape-mounted semiconductors may be stacked, and that the devices may be electrically interconnected through structures formed in vias in the insulative film. Mukerji fails, however, to teach or suggest a laminated structure wherein the ball terminals of an upper individual chip scale package are electrically connected to the circuit on an outer surface of the tape.

Crafts relates to a method for forming Pb/Sn bumps on a wafer for a C4 process. Crafts does not teach or suggest the use of a C4 process to attach the bond pads of a chip to an anisotropic conductive adhesive film by applying an anisotropic conductive adhesive on the tape and using a C4 process. Nor does Crafts cure Mukerji's deficiencies with respect to forming ball terminals on the surface of a tape of an anisotropic conductive adhesive film, or forming a laminated structure wherein the ball terminals of an upper individual chip scale package are electrically connected to the circuit on an outer surface of the tape.

Therefore, since both references are silent with respect to the use of a C4 process to attach the bond pads of a chip to an anisotropic conductive adhesive film by applying an anisotropic conductive adhesive on the tape and using a C4 process, forming ball terminals on the surface of a tape of an anisotropic conductive adhesive film, and forming a laminated structure wherein the ball terminals of an upper individual chip scale package are electrically connected to the circuit on an outer surface of the tape, no *prima facie* case of obviousness has been established with respect to Claim 1 and Claims dependent thereon.

Atty. Docket No. PIA31221/DBE/US
Serial No: 10/751,200

Thus Mukerji and Crafts fail to disclose all of the limitations of independent Claim 1. Claims 2 and 5-12 all depend on Claim 1. Therefore the rejection of Claims 1-2 and 5-12 under 35 U.S.C 103(a) as being unpatentable over Mukerji in view of Crafts is improper, and should be withdrawn.

Furthermore, the references themselves do not disclose, suggest, or motivate a person skilled in the art to combine Mukerji with Crafts to arrive at the present claimed invention. The Examiner states that "the method of forming a device is not germane to the issue of patentability of the device itself." (OA2, page 4, ll. 18-19.) However, Applicants respectfully note that the claims of the present invention are directed to a method, and not to a device. Therefore the steps of the method are precisely germane to the patentability of the method. Even if one could somehow construe the disclosures of the cited references broadly enough to suggest all of the claim limitations to one of ordinary skill of the art, the references do not motivate such a person to do so.

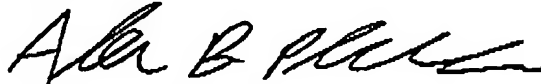
Conclusions

In view of the above amendments and remarks, all bases for objection and rejection are believed to be overcome, and the application is believed to be in condition for allowance. Early notice to that effect is earnestly requested.

Atty. Docket No. PIA31221/DBE/US
Serial No: 10/751,200

If it is deemed helpful or beneficial to the efficient prosecution of the present application,
the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,



Andrew D. Fortney, Ph.D.
Reg. No. 34,600

Alec B. Plumb
Reg. No. 56,433
THE LAW OFFICES OF ANDREW D. FORTNEY, PH.D., P.C.

7257 N. Maple Avenue, Suite 107
Fresno, California 93720
(559) 299 - 0128